CALIFORNIA STATE SCIENCE FAIR
2002 PROJECT SUMMARY

Name(s)
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Project Number
22225

Project Title
Partial Area Array Flip Chip Methodology and Automation

Abstract

Objectives/Goals
Design a methodology to assemble flip chips using standard IO circuits to maximize IO count and minimize implementation time. Develop the methodology to be usable with an existing core requiring IO placement or as a preliminary floor-planning tool. Automate the procedure to further reduce implementation time with self-explanatory graphical user interfaces (GUIs).

Methods/Materials
The program was written in the interpreted SKILL programming language in the Cadence Opus environment with IP from NurLogic Design, Inc. Terminals used were a local Windows 1998 machine (Intel Pentium II, 64 MB RAM) on a Unix network and a Windows XP machine (AMD Athlon 1.3GHz, 256 MB DDR RAM) remotely connected to the Unix network. This second terminal uses F-Secure SSH Tunnel and Terminal to gain access to the network. The processor-intensive operations were performed on various nodes with dual UltraSparq2 processors running Sun Solaris.

Results
Algorithms and methodology were developed and several routines were written to design double IO rings, the bump pad array and a multi-function power distribution mesh, capable of being used as a floor plan for a new chip or to conform to an existing core for flip chips. The methodology provides for roughly doubling the IO count, and the automation reduces design time by several orders of magnitude.

Conclusions/Discussion
Flip Chip technology has been increasing in popularity in recent years due to several electrical, mechanical, and thermal benefits. However, its growth has been limited by a lack of a cohesive methodology for rapid mass development of high IO count chips. Such a methodology, as this project attempts to create, has the potential to greatly expand the viability of flip chip.

Summary Statement
This project includes the development of methodology and its automation to rapidly design high IO count flip chips by using a partial area array and several new innovations such as a secondary IO ring.

Help Received
Technical support, funding and workspace provided by NurLogic Design, Inc.