CALIFORNIA STATE SCIENCE FAIR
2015 PROJECT SUMMARY

Name(s)

Vikram Bhagavatula

Project Number

J0904

Project Title

Dynamic Dataflow Processor (DDP)

Abstract

Objectives/Goals

To see if a scalable Dynamic Dataflow Processor architecture is faster compared to a conventional serial processor and a conventional parallel processor.

Methods/Materials

The materials used for this project was a hardware simulation\synthesis tool called ISE Webpack (a free tool provided by Xilinx). I used Verilog (a hardware description language) for modeling the RTL model of the micro-architecture and simulating my hardware architecture. For designing my architecture, I first created basic diagrams, block diagrams, timing diagrams, and pseudo-code. I then refined my architecture (and micro-architecture) based on all these models, and implemented this into Verilog. After that, I used the simulation tool to simulate my design and analyze, debug, and improve my architecture and micro-architecture. Then, for comparative analysis, I created a behavioral model for a conventional parallel processor and a conventional serial processor in Verilog. I then ran the simulations of all of them under several situations and compared their waveforms. I also changed the number of processors used in the testing to see its scalability (i.e. comparing how a certain number of conventional parallel processors, conventional serial processors, and DDP(s) performed on a larger task, etc.)

Results

The results were estimated that, on average, a single DDP was 4 times faster than a conventional serial processor and 2 times faster than a conventional parallel processor. An array of 4x4 DDP processors were estimated to be 16 times faster than a serial processor and approximately 2 times faster than conventional parallel processor.

Conclusions/Discussion

My conclusion for this project is that a scalable dynamic dataflow processor architecture is faster compared to a conventional parallel processor and a conventional serial processor.The DDP architecture has latency issues with the join or combining of results from other DDP processors in a network and may not be suitable for designs that need low latency or delay. Overall DDP is flexible and scalable to be implemented on chip level or board level with multiple DDP chips on a board.

I also realized, in this project, a systematic top-down methodology was extremely efficient and that behavioral modeling was a very powerful technique useful for this [top-down] approach.

Summary Statement

A parallel dynamic dataflow processor architecture (that is scalable) was developed to study whether this architecture would be faster compared to a conventional serial and a conventional parallel processor architecture.

Help Received

My father primarily guided me in understanding concepts in behavioral modeling , verilog coding, and free tools that could be used to work on this project. I extensively researched online reading articles on VLSI , parallel computing, Verilog RTL coding techniques,and example codes.